



STB57N65M5, STF57N65M5, STI57N65M5, STP57N65M5

N-channel 650 V, 0.056 Ω typ., 42 A MDmesh™ V Power MOSFET in I²PAK, TO-220, TO-220FP and D²PAK packages

Datasheet — production data

Features

Order codes	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STB57N65M5 STF57N65M5 STI57N65M5 STP57N65M5	710 V	< 0.063 Ω	42 A

- Worldwide best R_{DS(on)}*area amongst the silicon based devices
- Higher V_{DSS} rating, high dv/dt capability
- Excellent switching performance
- Easy to drive, 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

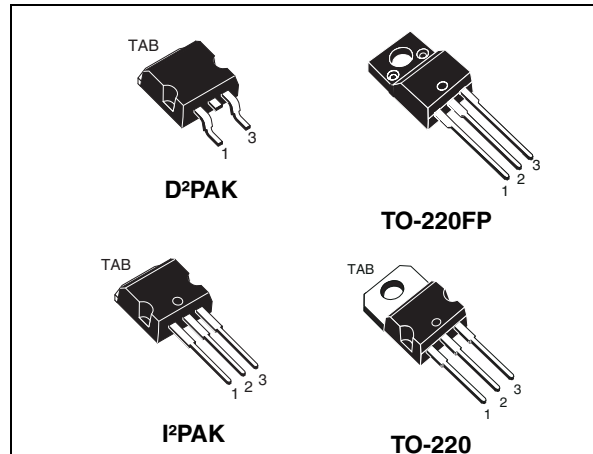


Figure 1. Internal schematic diagram

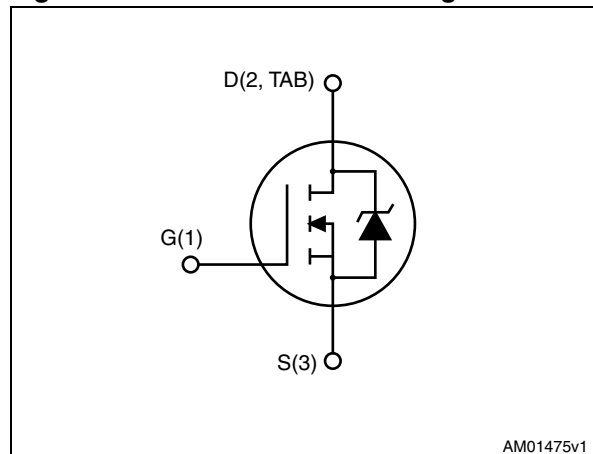


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB57N65M5 STF57N65M5 STI57N65M5 STP57N65M5	57N65M5	D ² PAK TO-220FP I ² PAK TO-220	Tape and reel Tube Tube Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, D ² PAK, I ² PAK	TO-220FP	
V _{GS}	Gate- source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	42	42 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	26.5	26.5 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	168	168 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	250	40	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{JMAX})	11		A
E _{AS}	Single pulse avalanche energy (starting T _j = 25°C, I _D = I _{AR} , V _{DD} = 50V)	960		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		2500	V
T _{stg}	Storage temperature	-55 to 150		°C
T _j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. I_{SD} ≤ 42 A, di/dt ≤ 400 A/μs, V_{Peak} < V_{(BR)DSS}, V_{DD} = 400 V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	I ² PAK	TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	0.50			3.1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5		62.5	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max ⁽¹⁾	30				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 21\text{ A}$		0.056	0.063	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	4200	-	pF
C_{oss}	Output capacitance			115		pF
C_{rss}	Reverse transfer capacitance			9		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0$ to 80% $V_{(BR)DSS}$	-	93	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related	$V_{GS} = 0$, $V_{DS} = 0$ to 80% $V_{(BR)DSS}$	-	303	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.3	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 21\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	98	-	nC
Q_{gs}	Gate-source charge			23		nC
Q_{gd}	Gate-drain charge			40		nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19)		73		ns
$t_{r(V)}$	Voltage rise time			15		ns
$t_{f(I)}$	Current fall time			12		ns
$t_{c(off)}$	Crossing time			19		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		42	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				168	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 42\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 19)	-	418		ns
Q_{rr}	Reverse recovery charge			8		μC
I_{RRM}	Reverse recovery current			40		A
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19)	-	528		ns
Q_{rr}	Reverse recovery charge			12		μC
I_{RRM}	Reverse recovery current			44		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK, I²PAK and TO-220

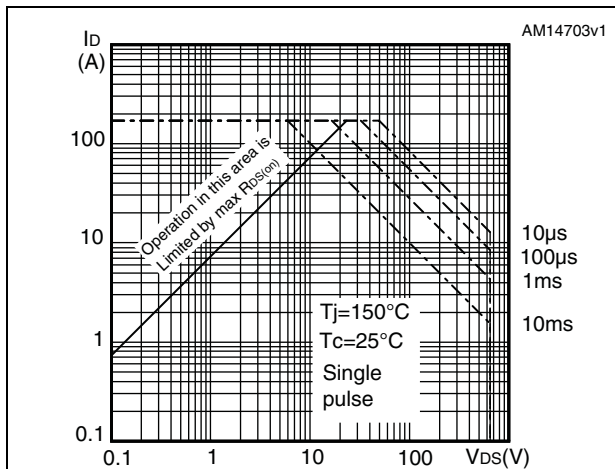


Figure 3. Thermal impedance for D²PAK, I²PAK and TO-220

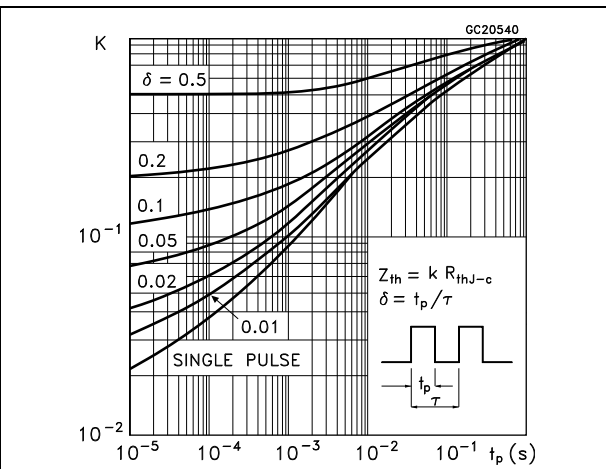


Figure 4. Safe operating area for TO-220FP

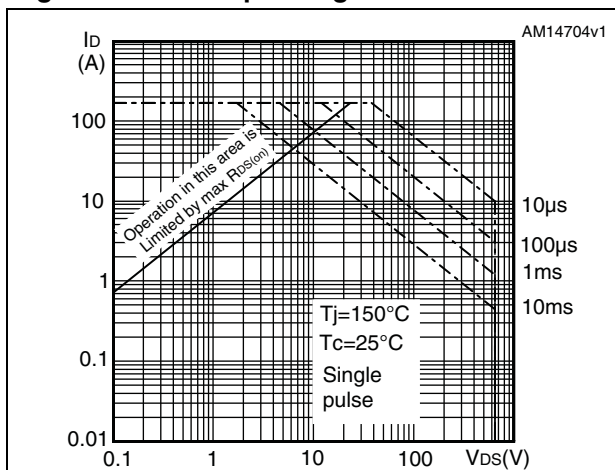


Figure 5. Thermal impedance for TO-220FP

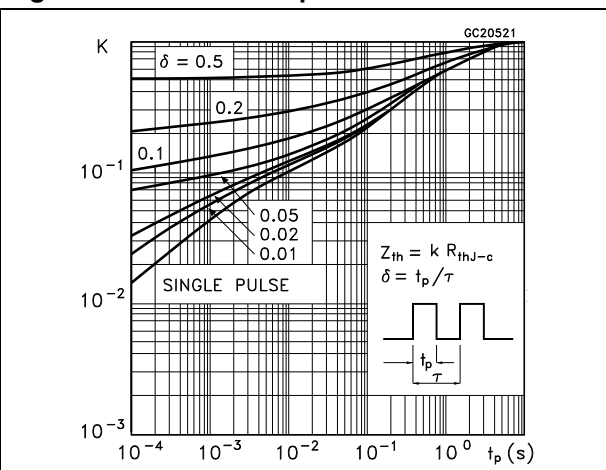


Figure 6. Output characteristics

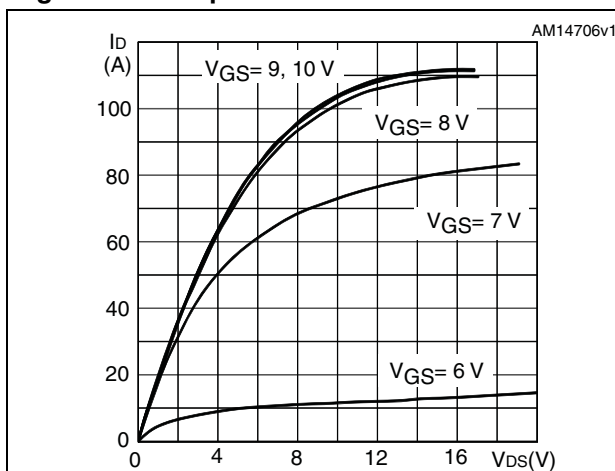


Figure 7. Transfer characteristics

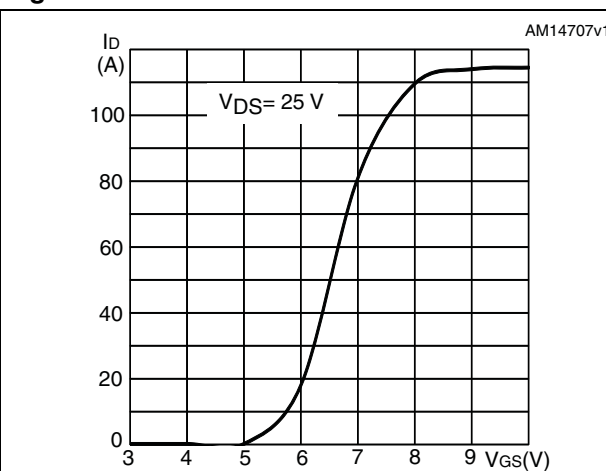


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on-resistance

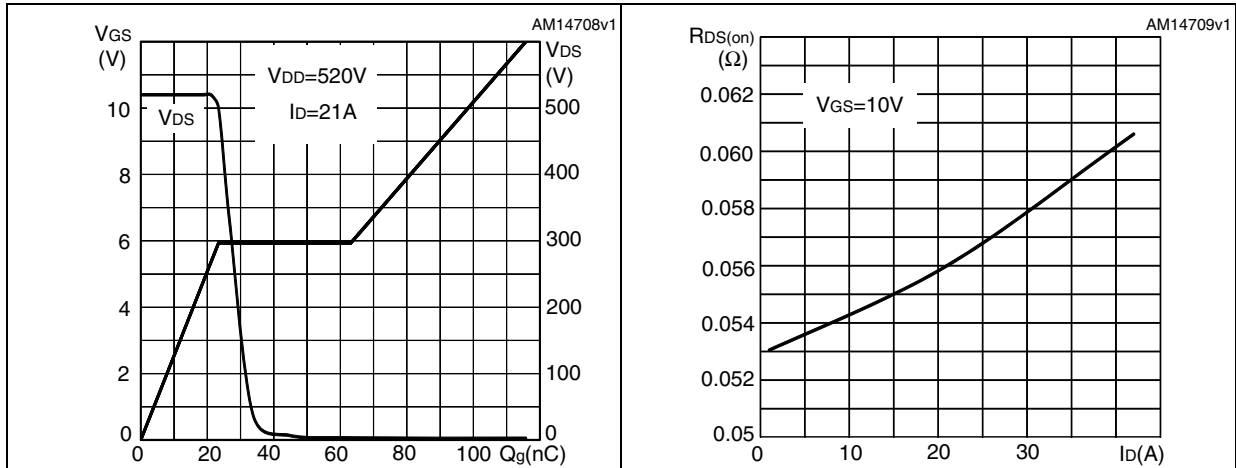


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

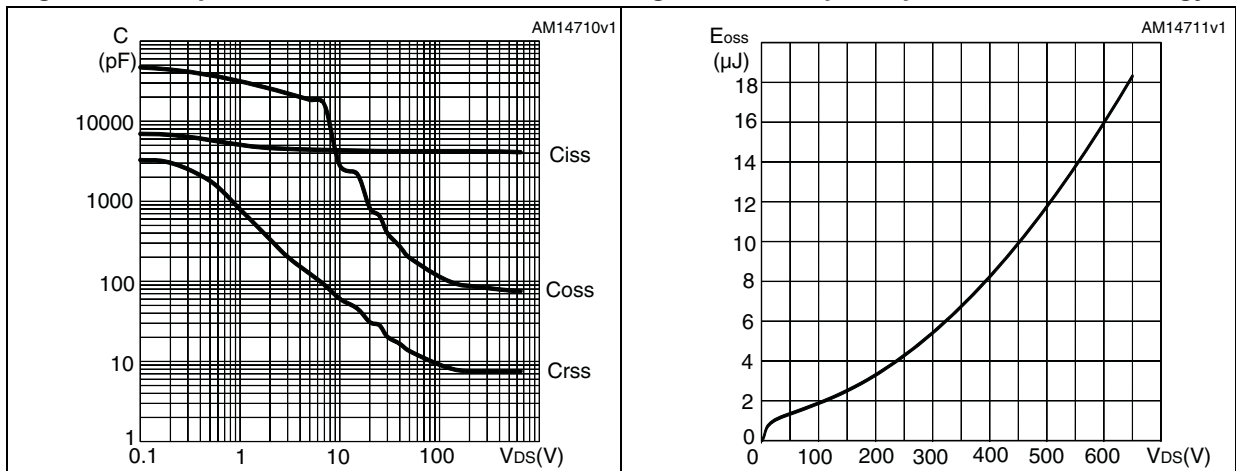


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on-resistance vs temperature

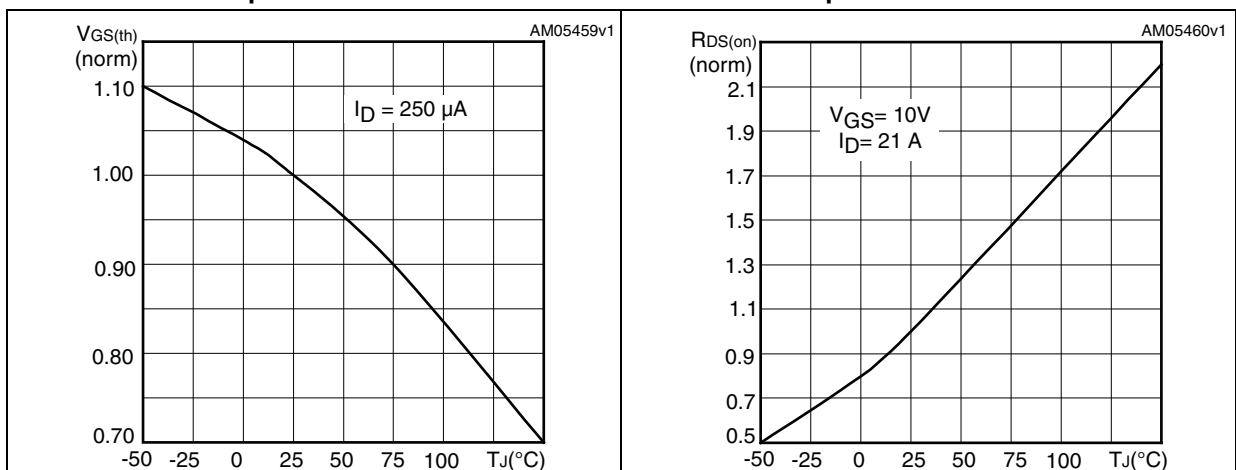


Figure 14. Source-drain diode forward characteristics

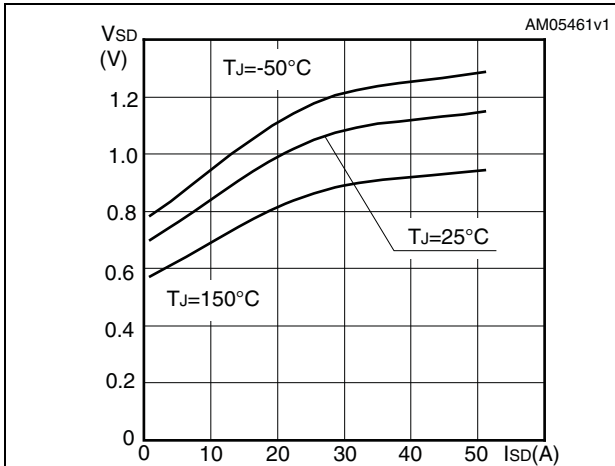


Figure 15. Normalized B_{VDSS} vs temperature

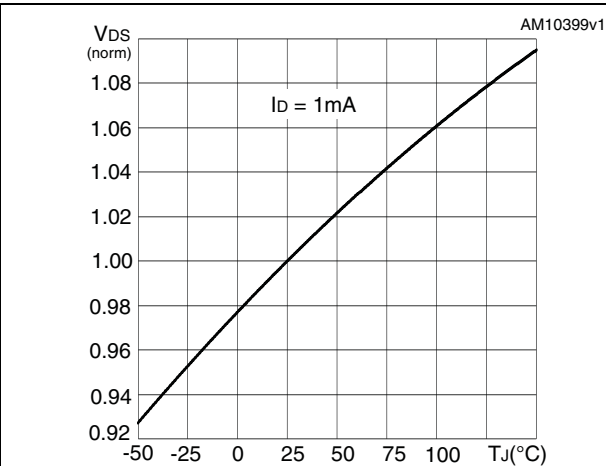
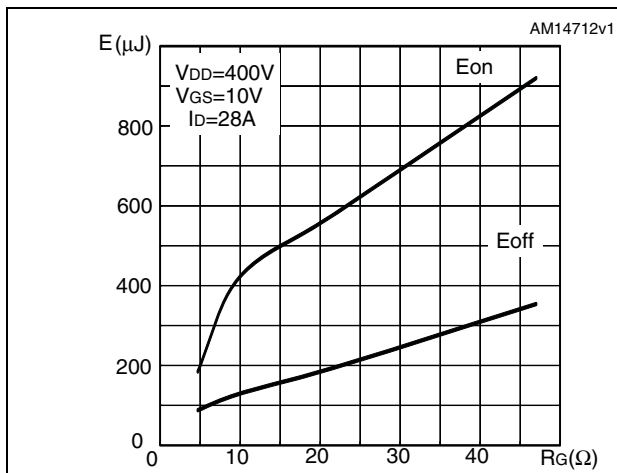


Figure 16. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 17. Switching times test circuit for resistive load



Figure 18. Gate charge test circuit

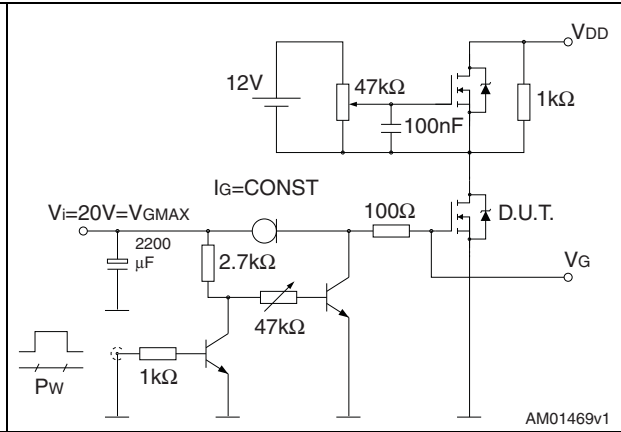


Figure 19. Test circuit for inductive load switching and diode recovery times

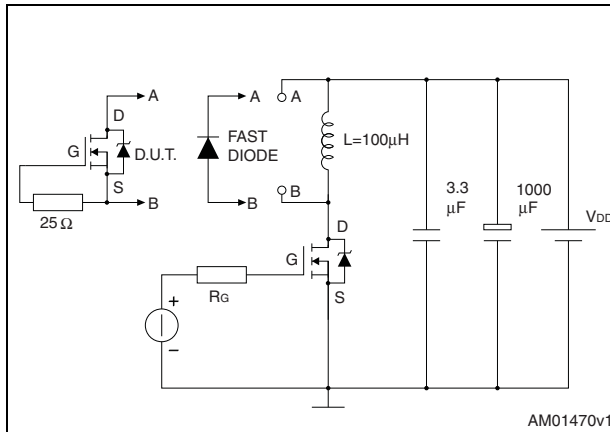


Figure 20. Unclamped inductive load test circuit

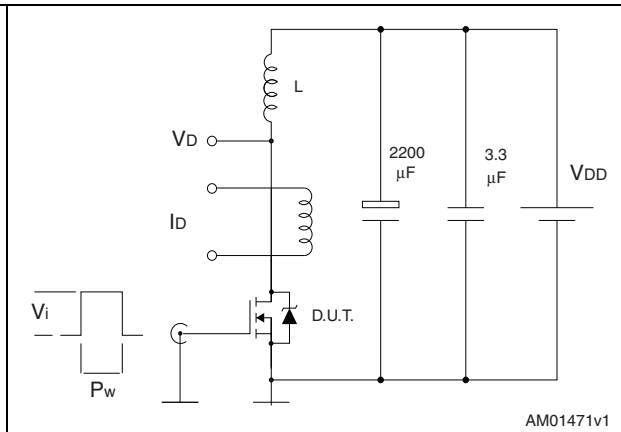


Figure 21. Unclamped inductive waveform

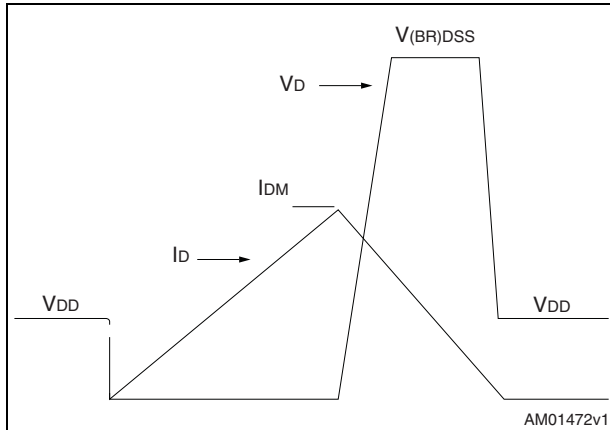
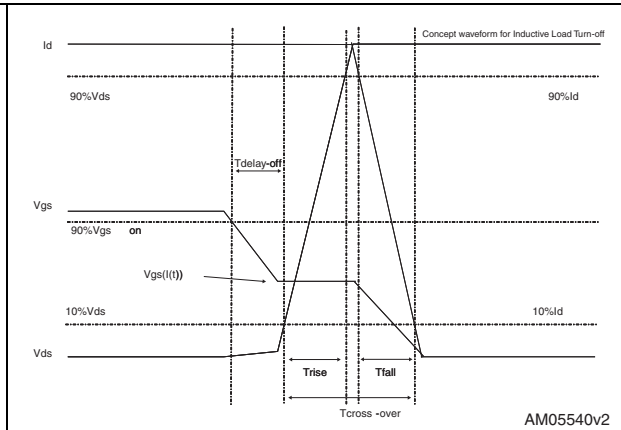


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

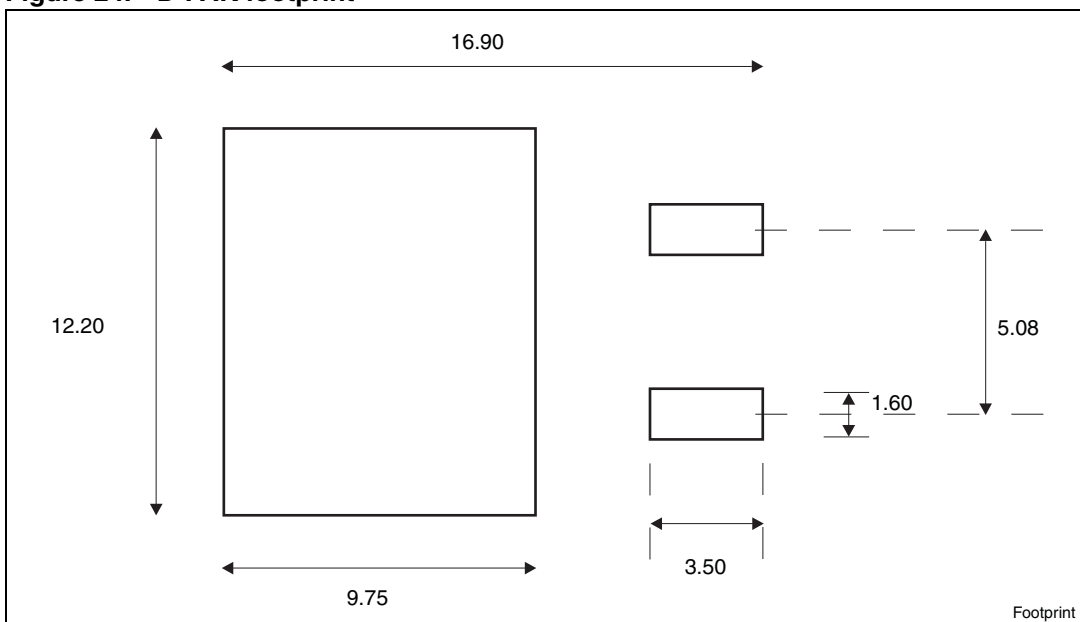
Table 8. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK (TO-263) drawing



Figure 24. D²PAK footprint^(a)

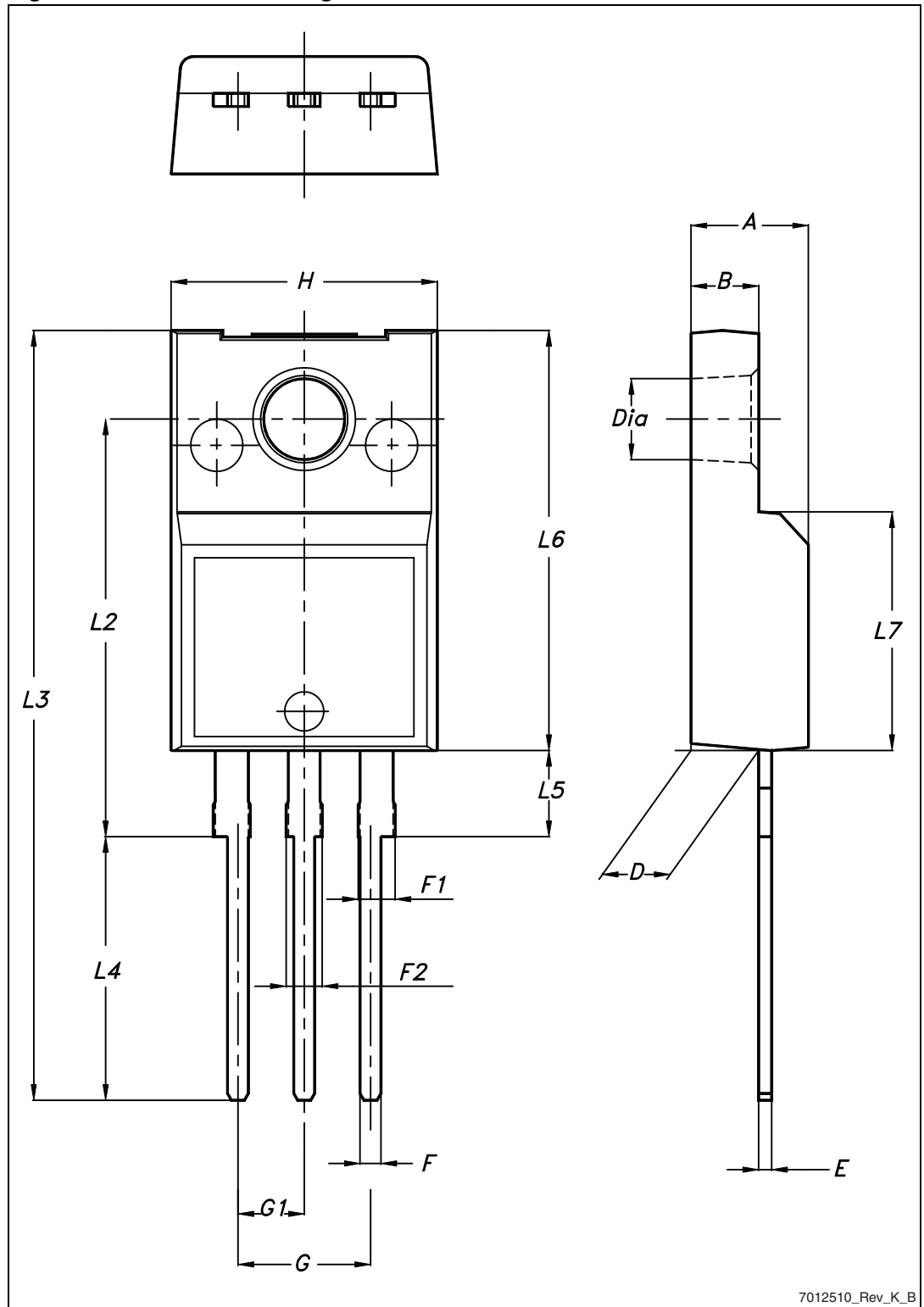


a. All dimension are in millimeters

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing



7012510_Rev_K_B

Table 10. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 26. I²PAK (TO-262) drawing

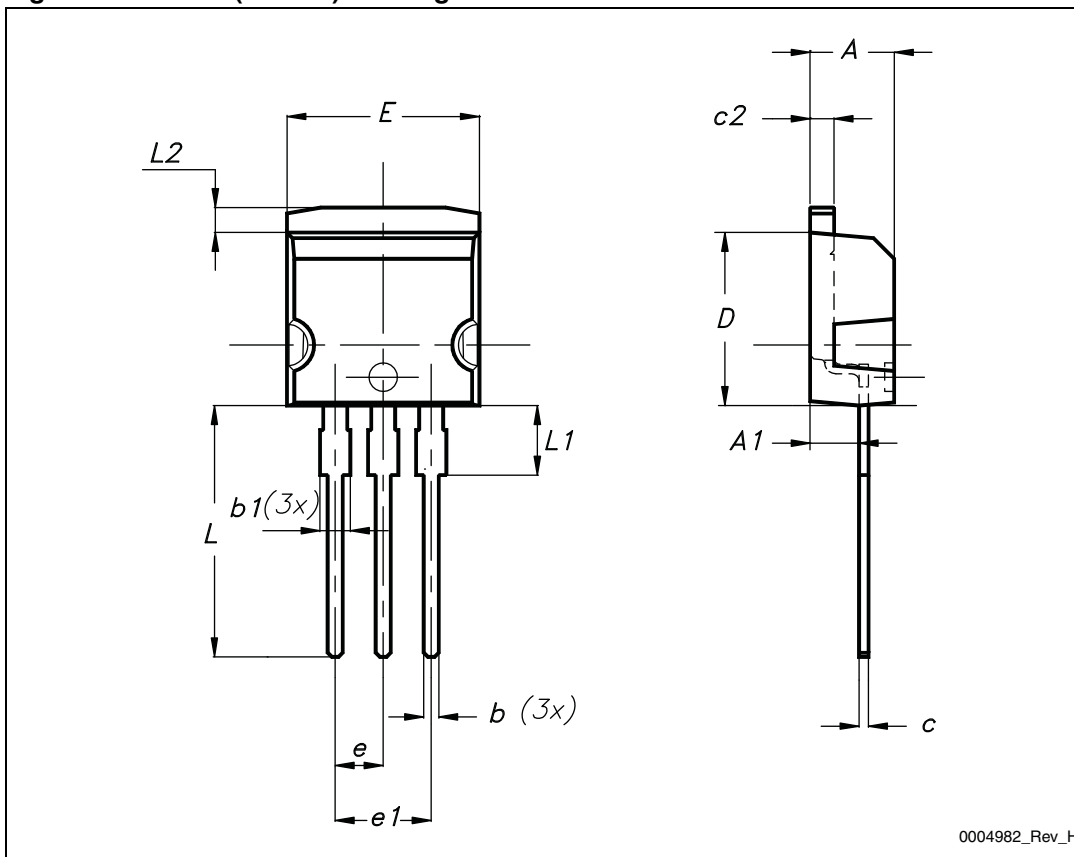
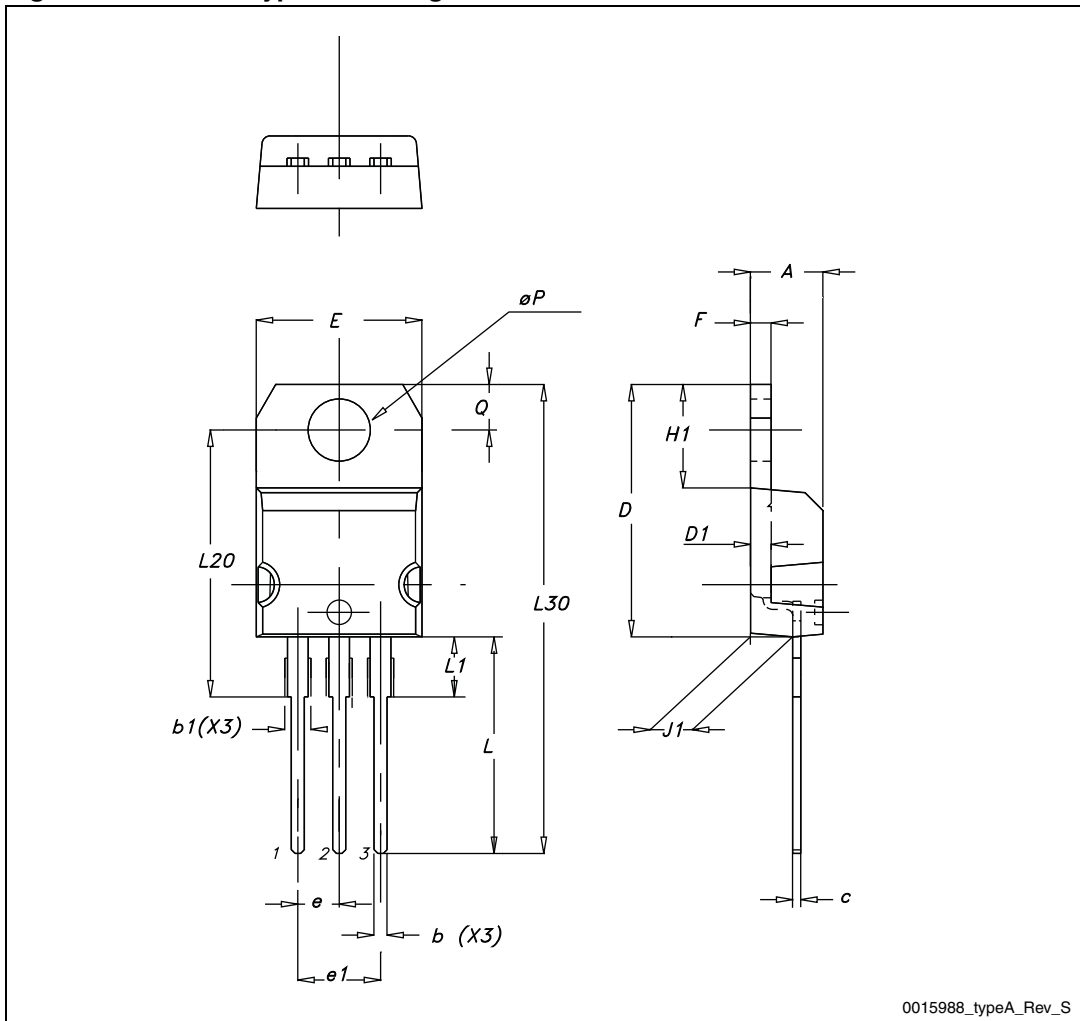


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

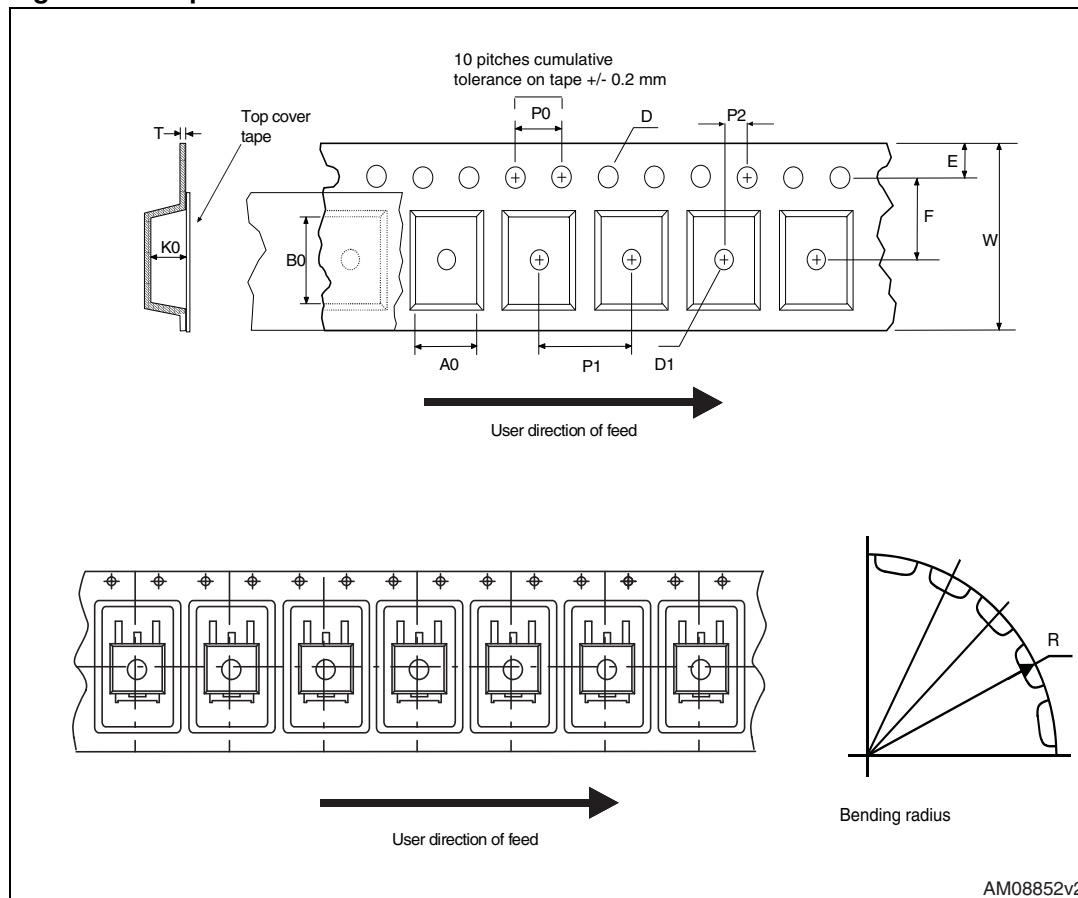


5 Packaging mechanical data

Table 12. D²PAK (TO-263) tape and reel mechanical data

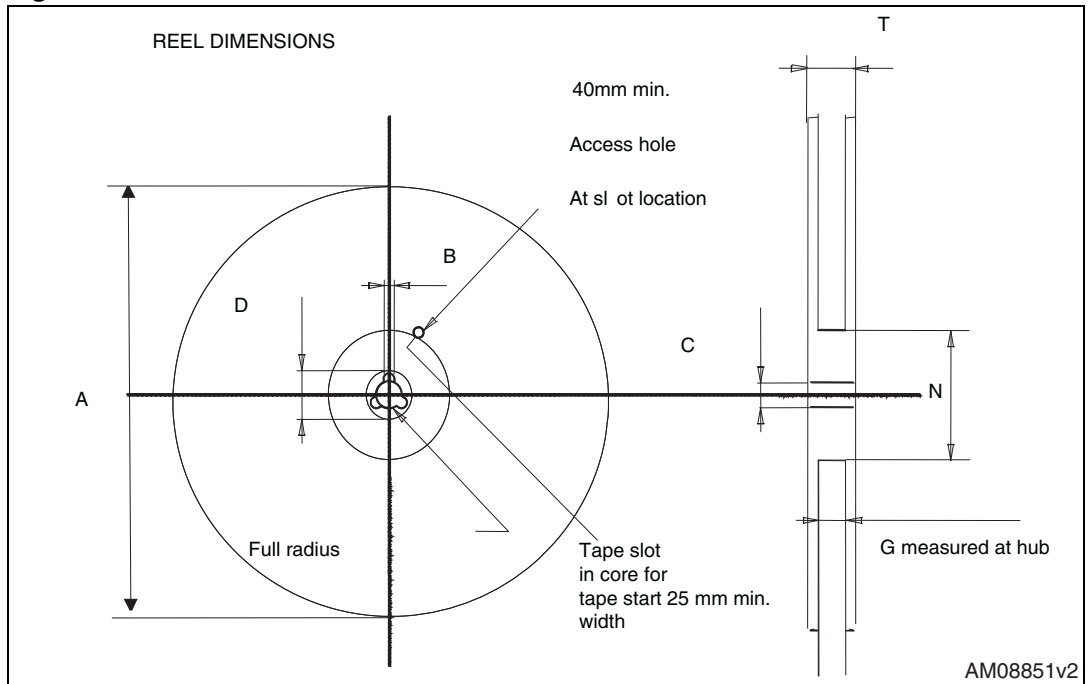
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 28. Tape



AM08852v2

Figure 29. Reel



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
06-Apr-2012	1	First release.
04-Jul-2012	2	Document status promoted from preliminary to production data. Added Section 2.1: Electrical characteristics (curves) .
21-Aug-2012	3	Updated symbols and parameters in Table 6: Switching times . Minor text change on the cover page.
04-Dec-2012	4	The part number STW57N65M5 has been moved to a separate datasheet.

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